



## TP2150B

### DUAL HIGH SIDE AND LOW SIDE MOSFET DRIVER

Technical Information

Revision 1.7 – June 2004

#### GENERAL DESCRIPTION

The TP2150B is a high speed, dual high side and low side MOSFET driver. The TP2150B level shifts CMOS or TTL input levels to gate signals for driving high voltage and high current MOSFETs in a dual half bridge or single full bridge configuration. The built in bootstrap circuitry allows for the high side to drive an N-channel power MOSFET.

#### Applications

- Switch mode audio power amplifier
- Switch mode power supply
- MOSFET driver

#### Benefits

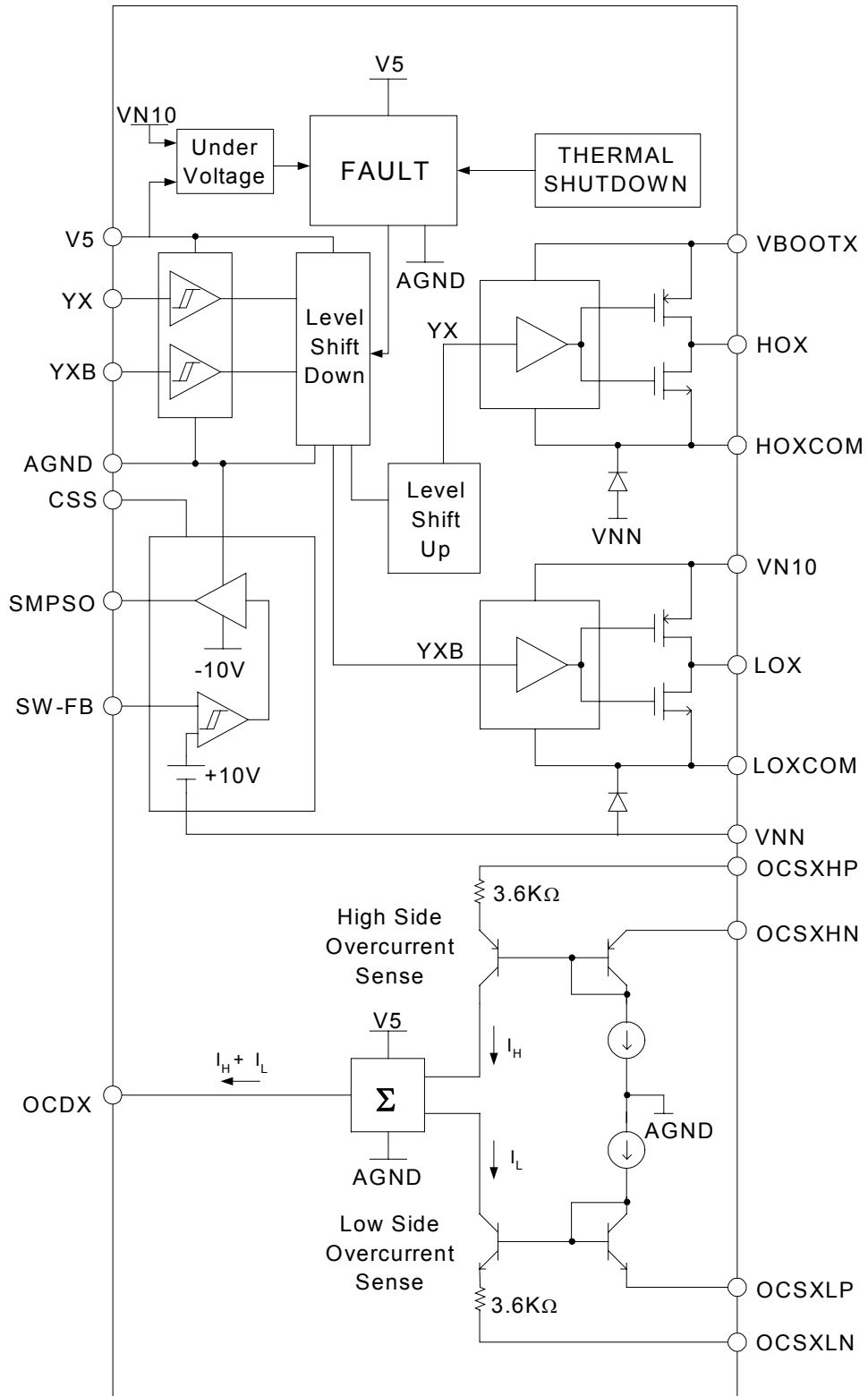
- Reduced system cost with smaller/less expensive power supply and heat sink
- Signal fidelity equal to high quality Class-AB amplifiers when paired with Tripath TC2001
- Floating reference high side driver allows for N channel output power MOSFETs on the high side.

#### Features

- Pin Compatible with Tripath TP2350B
- Supports wide range of power supplies
- Built in switching regulator driver to power the gate drive circuitry (VN10)
- Over-current protection
- Over-temperature protection



# BLOCK DIAGRAM



**Absolute Maximum Ratings TP2150B** (Note 3)

SYMBOL	PARAMETER	Value	UNITS
VPP, VNN	Supply Voltage	+/- 65	V
VN10	Voltage for FET drive	VNN+13	V
V5	5V power supply	6	V
T <sub>STORE</sub>	Storage Temperature Range	-55° to 150°	C
T <sub>A</sub>	Operating Free-air Temperature Range (Note 4)	-40° to 85°	C
T <sub>J</sub>	Junction Temperature	150°	C
ESD <sub>HB</sub>	ESD Susceptibility – Human Body Model (Note 5) All pins	2000	V
ESD <sub>MM</sub>	ESD Susceptibility – Machine Model (Note 6) All pins	200	V
V <sub>LOGIC</sub>	Voltage input on logic pins (pins 9,13,14,16,17)	-0.3 to (V5+0.3)	V
V <sub>OCSH</sub>	Voltage input on MOSFET high side overcurrent detect pins (pins 33,34,50,51)	VPP	V
V <sub>OCSL</sub>	Voltage input on MOSFET low side overcurrent detect pins (pins 30,31,53,54)	VNN	V
V <sub>BOOT</sub>	Voltage input on VBOOT1 and VBOOT2 pins (pins 27,57)	VPP+12	V

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

See the table below for Operating Conditions.

Note 4: This is a target specification. Characterization is still needed to validate this temperature range.

Note 5: Human body model, 100pF discharged through a 1.5KΩ resistor.

Note 6: Machine model, 220pF – 240pF discharged through all pins.

**Thermal Characteristics TP2150B**

SYMBOL	PARAMETER	Value	UNITS
θ <sub>JA</sub>	Junction-to-air Thermal Resistance	35°	C/W

**Electrical Characteristics TP2150B** (Note 7)

$T_A = 25\text{ }^\circ\text{C}$ . Unless otherwise noted, the supply voltage is  $V_{PP}=|V_{NN}|=45\text{V}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
$I_q$	Quiescent Current (No load, $BBM0=1, BBM1=0,$ Mute = 0V)	$V_{PP} = +45\text{V}$		30	55	mA
		$V_{NN} = -45\text{V}$ (using external VN10)		30	45	mA
		$V_{NN} = -45\text{V}$ (using SMPSO pin to drive IRFL9110 for generating VN10)		65	75	mA
		$V_{N10} = 10\text{V}$ $V_5 = 5\text{V}$		100 10.5	110 15	mA mA
$V_{IH}$	Logic High Input Voltage		$V_5-1$			V
$V_{IL}$	Logic Low Input Voltage				1	V
$I_{IN}$	Input Current for logic inputs			50	500	nA
$R_{DS}$	MOSFET On Resistance (high side)	$I_{OUT} = 50\text{mA}$ $V_{N10}=10\text{V}$		53		$\Omega$
$R_{DS}$	MOSFET On Resistance (low side)	$I_{IN} = 50\text{mA}$ $V_{N10}=10\text{V}$		2		$\Omega$
$I_{PK}$	Peak Output Current			200		mA
$Q_G$	Gate Charge Drive Capability			35		nC
$V_{OUT}$	Output Voltage for OCD pins	$V_{IN} = 0.5\text{V}$ between OCSXXX pins (i.e. pins 51 and 50, pins 53 and 54, pins 33 and 34, pins 30 and 31)	1.2	1.5		V
$I_{BIASOCD}$		$V_{IN} = 0\text{V}$ between OCSXXX pins (i.e. pins 51 and 50, pins 53 and 54, pins 33 and 34, pins 30 and 31)	10	20		$\mu\text{A}$

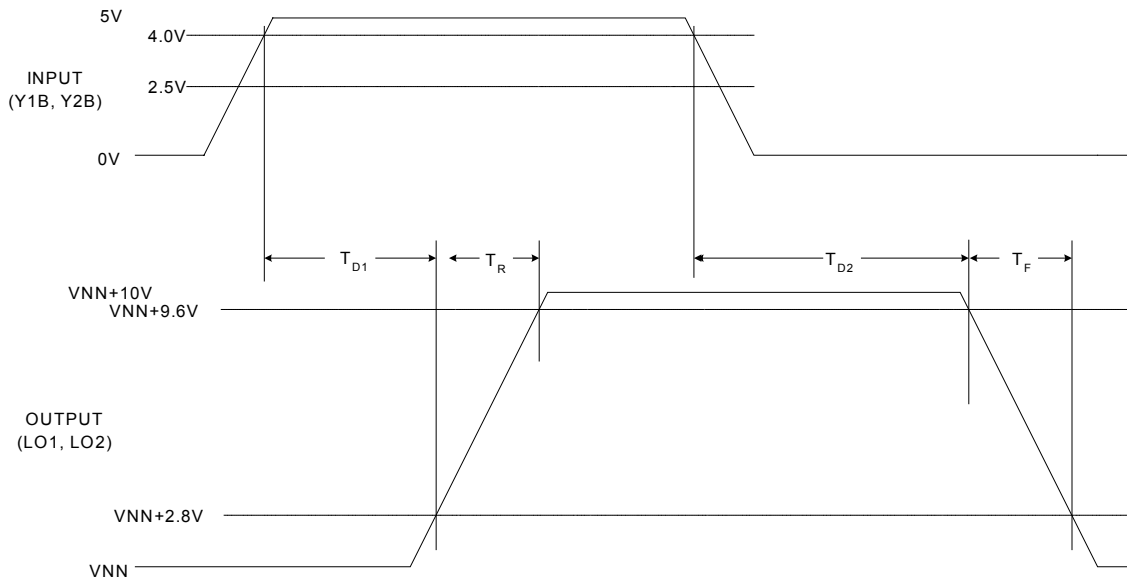
Note 7: Minimum and maximum limits are guaranteed but may not be 100% tested.

**Operating Conditions TP2150B** (Note 8)

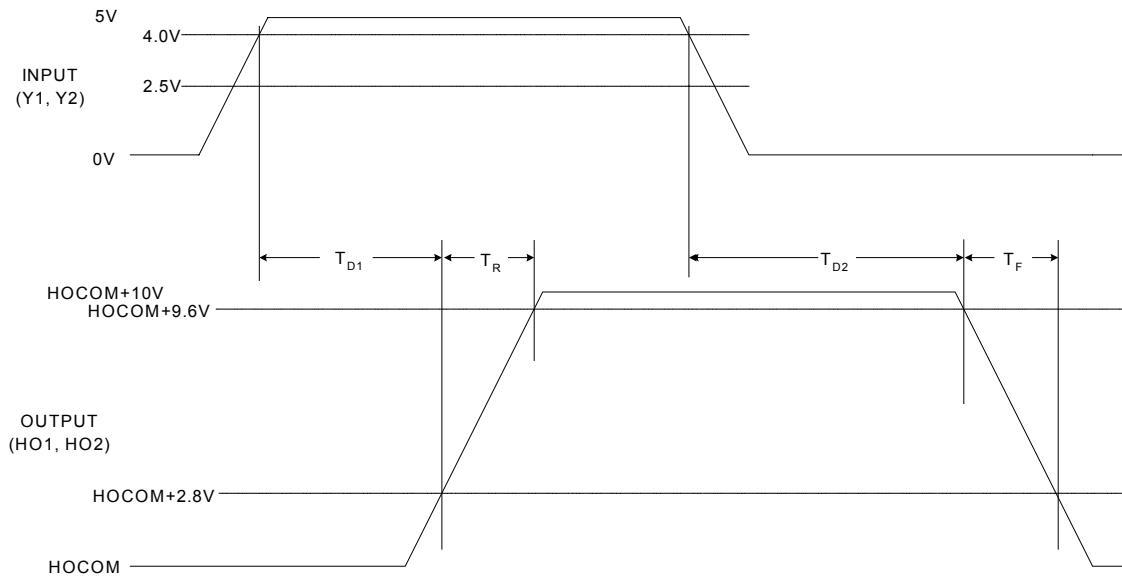
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
$V_{PP}, V_{NN}$	Supply Voltage	+/- 15	+/-45	+/- 65	V
VN10	Voltage for FET drive (Volts above VNN)	9	10	12	V
V5	5V power supply	4.5	5	5.5	V
$T_R$	Rise Time (Low Side Driver with no load)		8		nS
$T_F$	Fall Time (Low Side Driver with no load)		35		nS
$T_{D1}$	Rise Time Delay (Low Side Driver with no load)		190		nS
$T_{D2}$	Fall Time Delay (Low Side Driver with no load)		135		nS
$T_R$	Rise Time (High Side Driver with no load)		2		nS
$T_F$	Fall Time (High Side Driver with no load)		30		nS
$T_{D1}$	Rise Time Delay (High Side Driver with no load)		160		nS
$T_{D2}$	Fall Time Delay (High Side Driver with no load)		140		nS

Note 8: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

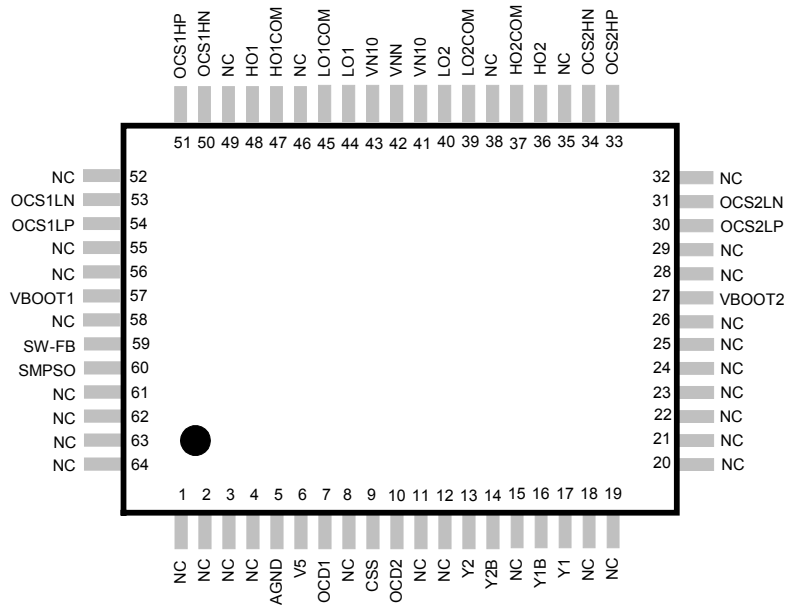
### Timing Diagram for Low Side Driver



### Timing Diagram for High Side Driver



# TP2150B Pinout

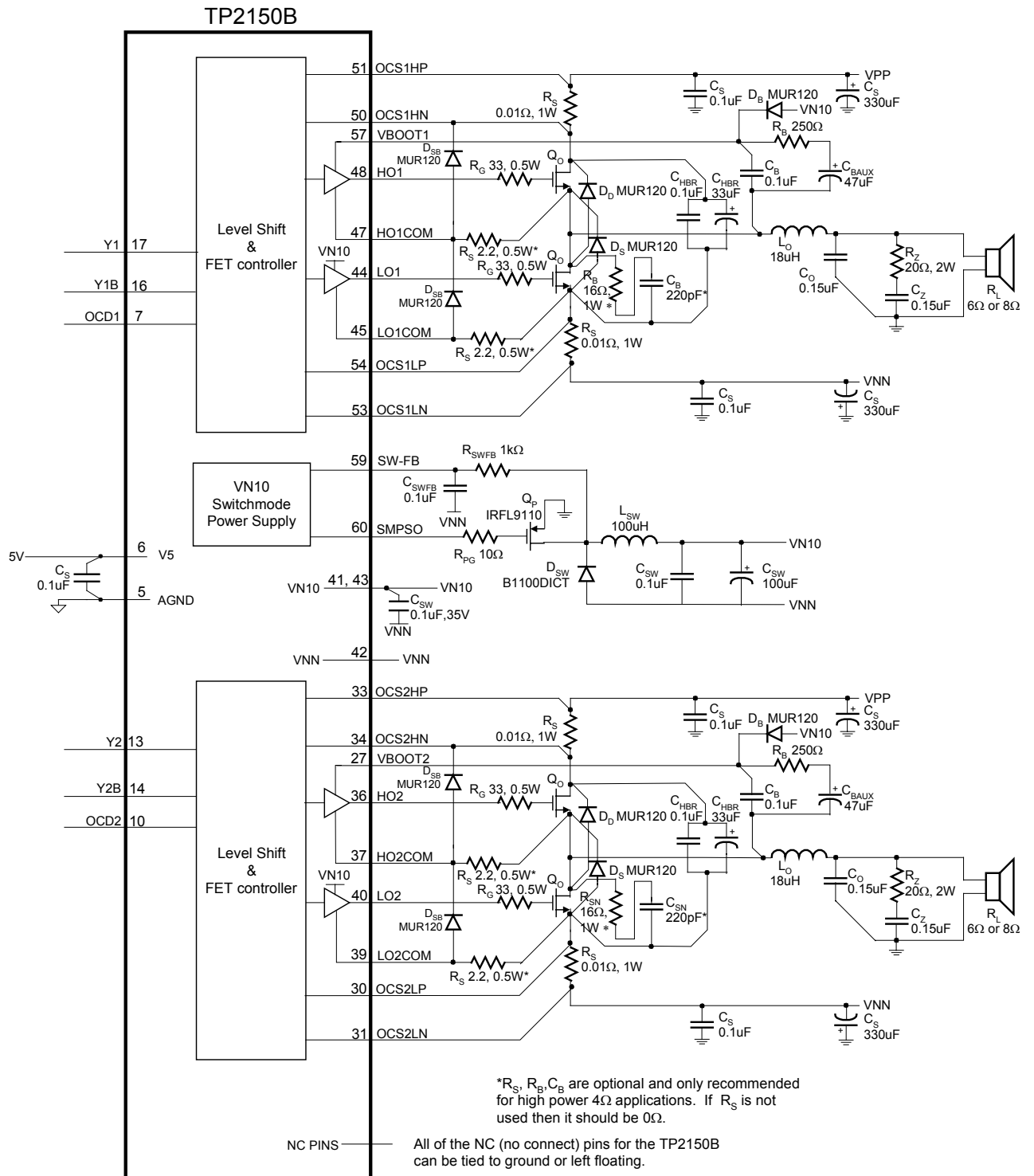


64-pin LQFP  
(Top View)

## TP2150B Pin Description

Pin	Function	Type	Description
5	AGND	Ground	Analog ground.
6	V5	Power	5V power supply input.
7	OCD1	Output	Over-current threshold adjustment (Channel 1)
9	CSS	Input (L)	Soft start control for VN10 regulator. Should be tied to +5V to enable VN10 generator
10	OCD2	Output	Over-current threshold adjustment (Channel 2)
13,17	Y2,Y1	Input (L)	Non-inverted switching modulator inputs
14,16	Y2B,Y1B	Input (L)	Inverted switching modulator inputs
27,57	VBOOT2, VBOOT1	Input	Bootstrapped voltage to supply drive to gate of high-side FET (Channel 2 & 1)
30,31	OCS2LP, OCS2LN	Input	Over Current Sense inputs, Channel 2 low-side
33,34	OCS2HP, OCS2HN	Input	Over Current Sense inputs, Channel 2 high-side
36,48	HO2,HO1	Output	High side gate drive output (Channel 2 & 1)
37,47	HO2COM, HO1COM	Output	Kelvin connection to source of high-side transistor (Channel 2 & 1)
39,45	LO2COM, LO1COM	Output	Kelvin connection to source of low-side transistor (Channel 2 & 1)
40,44	LO2,LO1	Output	Low side gate drive output (Channel 2 & 1)
41,43	VN10	Power	"Floating" supply input for the FET drive circuitry. This voltage must be stable and referenced to VNN.
42	VNN	Power	Negative supply voltage.
50,51	OCS1HN, OCS1HP	Input	Over Current Sense inputs, Channel 1 high-side
53,54	OCS1LN, OCS1LP	Input	Over Current Sense inputs, Channel 1 low-side
59	SW-FB	Input	Feedback for regulating switching power supply output for VN10
60	SMP SO	Output	Switching power supply output for VN10
1,2,3,4,8, 11,12,15, 18,19,20, 21,22,23, 24,25,26, 28,29,32, 35,38,46, 49,52,55, 56,58,61, 62,63,64	NC	NC	Not connected (bonded) internally.

## TP2150B Typical Application Circuit





**External Components Description** (Refer to the Application/Test Circuit)

Components	Description
D <sub>B</sub>	Bootstrap diode. This diode charges up the bootstrap capacitors when the output is low (at V <sub>NN</sub> ) to drive the high side gate circuitry. A fast or ultra fast recovery diode is recommended for the bootstrap circuitry. In addition, the bootstrap diode must be able to sustain the entire V <sub>PP</sub> -V <sub>NN</sub> voltage. Thus, for most applications, a 150V (or greater) diode should be used.
C <sub>B</sub>	High frequency bootstrap capacitor, which filters the high side gate drive supply. This capacitor must be located as close to V <sub>BOOT1</sub> (pin 57 of the TP2150B) or V <sub>BOOT2</sub> (pin 27 of the TP2150B) for reliable operation. The “negative” side of C <sub>B</sub> should be connected directly to the HO1COM (pin 47 of the TP2150B) or HO2COM (pin 37 of the TP2150B). Please refer to the Application / Test Circuit.
C <sub>BAUX</sub>	Bulk bootstrap capacitor that supplements C <sub>B</sub> during “clipping” events, which result in a reduction in the average switching frequency.
R <sub>B</sub>	Bootstrap resistor that limits C <sub>BAUX</sub> charging current during TP2150B power up (bootstrap supply charging).
C <sub>S</sub>	Supply decoupling for the power supply pins. For optimum performance, these components should be located close to the TP2150B and returned to ground.
R <sub>S</sub>	Over-current sense resistor. Please refer to the section, Setting the Over-current Threshold, in the Application Information for a discussion of how to choose the value of R <sub>S</sub> to obtain a specific current limit trip point.
C <sub>HBR</sub>	Supply decoupling for the high current Half-bridge supply pins. These components must be located as close to the output MOSFETs as possible to minimize output ringing which causes power supply overshoot. By reducing overshoot, these capacitors maximize both the TP2150B and output MOSFET reliability. These capacitors should have good high frequency performance including low ESR and low ESL. In addition, the capacitor rating must be twice the maximum V <sub>PP</sub> voltage. Panasonic EB capacitors are ideal for the bulk storage (nominally 33uF) due to their high ripple current and high frequency design.
R <sub>G</sub>	Gate resistor, which is used to control the MOSFET rise/ fall times. This resistor serves to dampen the parasitics at the MOSFET gates, which, in turn, minimizes ringing and output overshoots. The typical power rating is 1/2 watt.
C <sub>Z</sub>	Zobel capacitor, which in conjunction with R <sub>Z</sub> , terminates the output filter at high frequencies. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs.
R <sub>Z</sub>	Zobel resistor, which in conjunction with C <sub>Z</sub> , terminates the output filter at high frequencies. The combination of R <sub>Z</sub> and C <sub>Z</sub> minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with increasing frequency. Depending on the program material, the power rating of R <sub>Z</sub> may need to be adjusted. The typical power rating is 2 watts.
L <sub>O</sub>	Output inductor, which in conjunction with C <sub>O</sub> , demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$ .
C <sub>O</sub>	Output capacitor, which, in conjunction with L <sub>O</sub> , demodulates (filters) the switching waveform into an audio signal. Forms a second order low-pass filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$ . Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs.

$D_D$	Drain diode. This diode must be connected from the drain of the high side output MOSFET to the drain of the low side output MOSFET. This diode absorbs any high frequency overshoots caused by the output inductor $L_O$ during high output current conditions. In order for this diode to be effective it must be connected directly to the drains of both the top and bottom side output MOSFET. A fast or ultra fast recovery diode that can sustain the entire VPP-VNN voltage should be used here. In most applications a 150V or greater diode must be used.
$D_S$	Source diode. This diode must be connected from the source of the high side output MOSFET to the source of the low side output MOSFET. This diode absorbs any high frequency undershoots caused by the output inductor $L_O$ during high output current conditions. In order for this diode to be effective it must be connected directly to the sources of both the top and bottom sides output MOSFETs. A fast or ultra fast recovery diode that can sustain the entire VPP-VNN voltage should be used here. In most applications a 150V or greater diode must be used.
$R_{PG}$	Gate resistor for the output MOSFET for the switchmode power supply. Controls the rise time, fall time, and reduces ringing for the gate of the output MOSFET for the switchmode power supply.
$Q_B$	Output MOSFET for the switchmode power supply to generate the VN10. This output MOSFET must be a P channel device.
$D_{SW}$	Flywheel diode for the internal VN10 buck converter. This diode also prevents VN10SW from going more than one diode drop negative with respect to VNN. This diode should be a Schottky or ultrafast rectifier.
$L_{SW}$	VN10 generator filter inductor. This inductor should be sized appropriately so that $L_{SW}$ does not saturate, and VN10 does not overshoot with respect to VNN during TP2150B turn on.
$C_{SW}$	VN10 generator filter capacitors. The high frequency capacitor (0.1uF) must be located close to the VN10 pins (pin 41 and 43 of the TP2150B) to maximize device performance. The bulk capacitor (100uF) should be sized appropriately such that the VN10 voltage does not overshoot with respect to VNN during TP2150B turn on.
$R_{SWFB}$	VN10 generator feedback resistor. This resistor sets the nominal VN10 voltage. With $R_{SWFB}$ equal to 1k $\Omega$ , the VN10 voltage generated will typically be 10V above VNN.
$C_{SWFB}$	VN10 generator feedback capacitor. This capacitor, in conjunction with $R_{SWFB}$ , filters the VN10 feedback signal such that the loop is unconditionally stable.
$D_{SB}$	HOCOM diode. These diodes must be connected from the HOCOM pin (pin 37 or pin 47 of the TP2150B) to the OCSHN pins (pin 34 or pin 50 of the TP2150B) and the OCSLP pins (pin 30 or 54 of the TP2150B). This diode absorbs any high frequency undershoots caused by the output inductor $L_O$ during high output current conditions and protects the TP2150B during these conditions. In order for this diode to be effective it must be connected directly to the HOCOM, OCSHN, and OCSLP pins of the TP2150B. A fast or ultra fast recovery diode that can sustain the entire VPP-VNN voltage should be used here. In most applications a 150V or greater diode must be used.
$C_{SN}$	High frequency snubber capacitor works as a low pass filter in conjunction with $R_{SN}$ to remove high frequency ringing components due to over/undershoot on the output switching waveform.
$R_{SN}$	High frequency snubber resistor works as a low pass filter in conjunction with $C_{SN}$ to remove high frequency ringing components due to over/undershoot on the output switching waveform.

## Application Information

### Overcurrent Protection

The TP2150B has over-current protection circuitry to protect itself and the output MOSFETs from short-circuit conditions. The TP2150B uses the voltage across a resistor  $R_S$  (measured via OCS1HP, OCS1HN, OCS1LP and OCS1LN for channel 1 of the TP2150B) that is in series with each output MOSFET to detect an over-current condition.  $R_S$  and  $R_{OCR}$  are used to set the over-current threshold. The OCS pins must be Kelvin connected for proper operation.

The TP2150B has overcurrent sense pins for both the high side output MOSFETs and the low side output MOSFETs. The OCSXHP and OCSXHN pins (pins 33 and 34, pins 50 and 51) sense the amount of current flowing out of the high side MOSFET. The OCSXLP and OCSXLN pins (pins 30 and 31, pins 53 and 54) sense the amount of current flowing into the low side MOSFET. These pins sense the voltage across a low resistance value resistor ( $R_S$ ) and this voltage is gained up and reflected at OCD1 (pin7) for channel 1. The OCD pins can be used to trigger an overcurrent condition at the output MOSFETs and then turn off the processor.

### Setting Over-current Threshold

$R_S$  and  $R_{OCR}$  determine the value of the over-current threshold,  $I_{SC}$ :

$$I_{SC} = 3580 \times (V_{TOC} - I_{BIAS} \times R_{OCR}) / (R_{OCR} \times R_S)$$

$$R_{OCR} = (3580 \times V_{TOC}) / (I_{SC} \times R_S + 3580 \times I_{BIAS})$$

where:

$R_S$  and  $R_{OCR}$  are in  $\Omega$

$V_{TOC}$  = Over-current sense threshold voltage for the processor  
= 1.0V (typically for the Tripath TC2000 and TC2001)

$I_{BIAS} = 20\mu A$

For example, to set an  $I_{SC}$  of 4.73A,  $R_{OCR} = 30.1k\Omega$  and  $R_S$  will be  $10m\Omega$ .

As high-wattage resistors are usually only available in a few low-resistance values ( $10m\Omega$ ,  $25m\Omega$  and  $50m\Omega$ ),  $R_{OCR}$  can be used to adjust for a particular over-current threshold using one of these values for  $R_S$ .

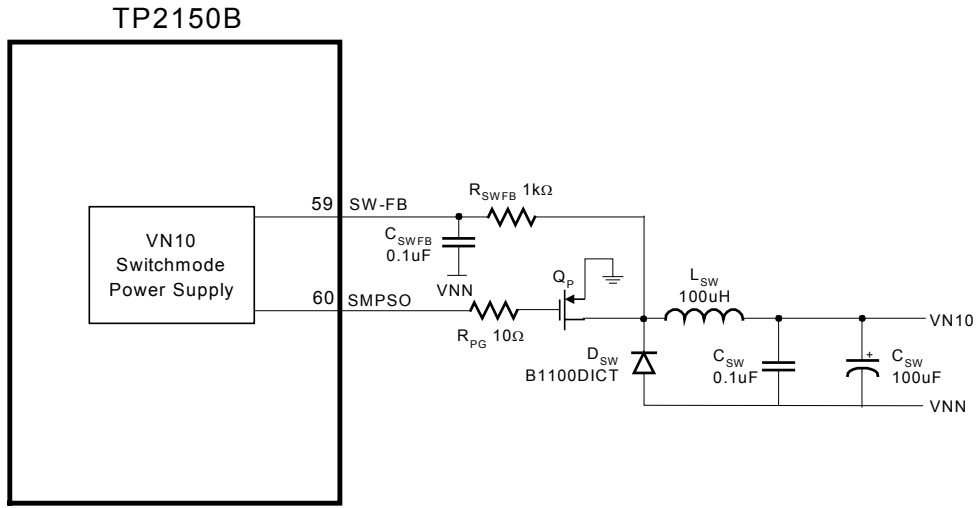
It should be noted that the addition of the bulk  $C_{HBR}$  capacitor shown in the Application / Test Diagram will increase the  $I_{SC}$  level. Thus, it will be larger than the theoretical value shown above. With  $C_{HBR}$  as shown in the typical application circuit, and with  $R_{OCR} = 30.1k\Omega$  and  $R_S = 10m\Omega$ , the typical current trip point is 7A. Once the designer has settled on a layout and specific  $C_{HBR}$  value, the system  $I_{SC}$  trip point can be adjusted by increasing the  $R_{OCR}$  value. The  $R_{OCR}$  should be increased to a level that allows expected range of loads to be driven well into clipping without current limiting while still protecting the output MOSFETs in case of a short circuit condition.

### VN10 Supply and Switch Mode Power Supply Controller

VN10 is an additional supply voltage required by the TP2150B. VN10 must be 10 volts more positive than the nominal VNN. VN10 must track VNN. Generating the VN10 supply requires some care.

The proper way to generate the voltage for VN10 is to use a 10V-positive supply voltage referenced to the VNN supply. The TP2150B has an internal switch mode power supply controller which generates the necessary floating power supply for the MOSFET driver stage in the TP2150B (nominally 10V with the external components shown in Application / Test Circuit). The SMP50 pin (pin 60) provides a switching output waveform to drive the gate of a P channel MOSFET. The source of the P channel MOSFET should be tied to power ground and the drain of the MOSFET should be tied to the VN10 through a 100uH inductor. Tripath recommends using

the internal VN10 generator to power the TP2150B. Figure 6 shows how the VN10 generator should be connected.

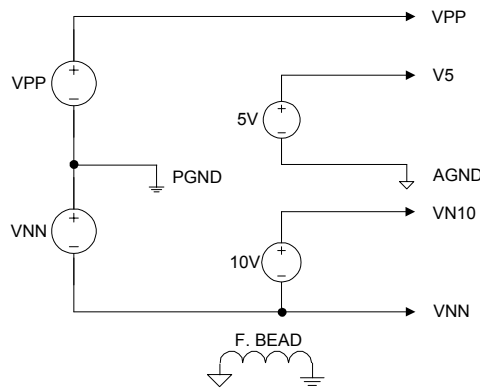


**Figure 6: VN10 Generator**

In some cases, though, a designer may wish to use an external VN10 generator. The specification for VN10 quiescent current (100mA typical) in the Electrical Characteristics section states the amount of current needed when an external floating supply is used. If the internal VN10 generator is not used then short the CSS pin to (pin 9) disable this feature.

One apparent method to generate the VN10 supply voltage is to use a negative IC regulator to drop PGND down to 10V (relative to VNN). This method will not work since negative regulators only sink current into the regulator output and will not be capable of sourcing the current required by VN10. Furthermore, problems can arise since VN10 will not track movements in VNN. The external VN10 supply must be able to source a minimum of 200mA into the VN10 pin. Thus, a positive supply must be used and must be referenced to the VNN rail. If the external VN10 supply does not track fluctuations in the VNN supply or is not able to source current into the VN10 pin, the TP2150B will not work and can also become permanently damaged.

Figure 7 shows the correct way to power the TP2150B:



**Figure 7: Proper Power Supply Connection**

### Output Transistor Selection

The key parameters to consider when selecting what MOSFET to use with the TP2150B are drain-source breakdown voltage (BV<sub>DSS</sub>), gate charge (Q<sub>g</sub>), and on-resistance (R<sub>DS(ON)</sub>).

The BV<sub>DSS</sub> rating of the MOSFET needs to be selected to accommodate the voltage swing between V<sub>SPOS</sub> and V<sub>SNEG</sub> as well as any voltage peaks caused by voltage ringing due to switching transients. With a 'good' circuit board layout, a BV<sub>DSS</sub> that is 50% higher than the V<sub>PP</sub> and V<sub>NN</sub> voltage swing is a reasonable starting point. The BV<sub>DSS</sub> rating should be verified by measuring the actual voltages experienced by the MOSFET in the final circuit.

Ideally a low Q<sub>g</sub> (total gate charge) and low R<sub>DS(ON)</sub> are desired for the best amplifier performance. Unfortunately, these are conflicting requirements since R<sub>DS(ON)</sub> is inversely proportional to Q<sub>g</sub> for a typical MOSFET. The design trade-off is one of cost versus performance. A lower R<sub>DS(ON)</sub> means lower I<sup>2</sup>R<sub>DS(ON)</sub> losses but the associated higher Q<sub>g</sub> translates into higher switching losses (losses = Q<sub>g</sub> x 10 x 1.2MHz). A lower R<sub>DS(ON)</sub> also means a larger silicon die and higher cost. A higher R<sub>DS(ON)</sub> means lower cost and lower switching losses but higher I<sup>2</sup>R<sub>DS(ON)</sub> losses.

### Gate Resistor Selection

The gate resistors, R<sub>G</sub>, are used to control MOSFET switching rise/fall times and thereby minimize voltage overshoots. They also dissipate a portion of the power resulting from moving the gate charge each time the MOSFET is switched. If R<sub>G</sub> is too small, excessive heat can be generated in the driver. Large gate resistors lead to slower MOSFET switching, which can lead to higher idle current.

### Recommended MOSFETs

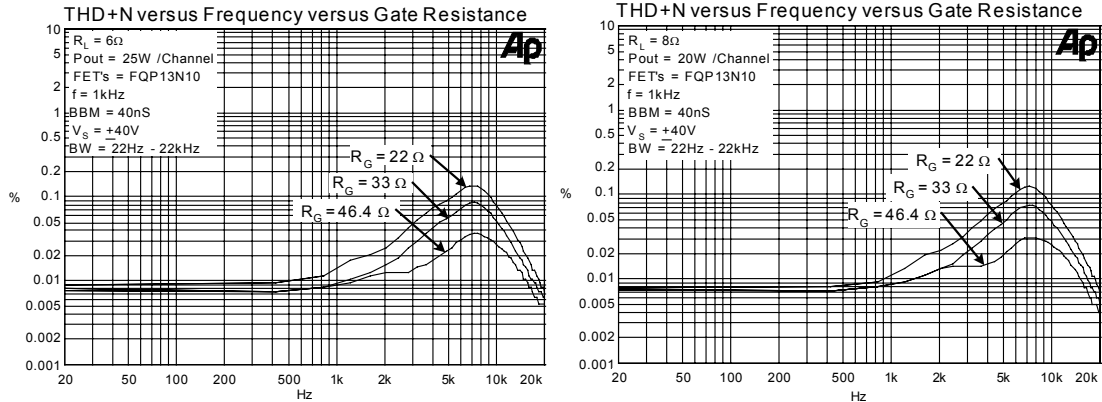
The following devices are capable of achieving full performance, both in terms of distortion and efficiency, for the specified load impedance and voltage range.

#### **Device Information – Recommended MOSFETs**

Part Number	Manufacturer	BV <sub>DSS</sub> (V)	I <sub>D</sub> (A)	Q <sub>g</sub> (nC)	R <sub>DS(on)</sub> (Ω)	P <sub>D</sub> (W)	Package
IRF520N	International Rectifier	100	9.7	25(max.)	0.20 (max.)	48	TO220
FQP13N10	Fairchild Semiconductor	100	12.8	12	0.142	65	TO220
STP14NF10	ST Microelectronics	100	14	15.5	0.16	60	TO220
IRF530N	International Rectifier	100	17	37(max.)	0.09 (max.)	70	TO220
BUK7575-100A	Philips Semiconductor	100	23	25	0.064	99	TO220
STP24NF10	ST Microelectronics	100	26	30	0.055	85	TO220
FQP16N15	Fairchild Semiconductor	150	16.4	23	0.123	108	TO220
FQP19N10	Fairchild Semiconductor	100	19	19	0.1	75	TO220
FDP2572	Fairchild Semiconductor	150	29	27	0.045	135	TO220

Note: The devices are listed in ascending current capability not in order of recommendation.

The following information represents qualitative data from system development using the TP2150B along with the Tripath TC2001 processor and the associated MOSFETs. Recommendations such as maximum supply voltages and gate resistor values are dependent on the PCB layout and component location. The gate resistor values were chosen to achieve about 18-80mA of idle current from the V<sub>PP</sub> supply. This value of supply current is a good compromise between low power efficiency and high frequency THD+N performance. As shown in Table 2 below, increasing the gate resistor value will improve high frequency THD+N performance at the expense of idle current draw. The BBM setting was 40nS in all cases. It should be understood that different MOSFETs will have different characteristics and will require some adjustment to the gate resistor to achieve the same idle current.



6 ohm and 8 ohm plots of THD+N versus Frequency for various gate resistor values

	6 ohms	8 ohms
22 ohms	18mA	18mA
33 ohms	20mA	20mA
46.4 ohms	80mA	80mA

Table 2: Idle current draw for VPP with various gate resistor values

**Application Information – Recommended MOSFETs**

Part Number	Recommended Max Supply Voltage	Typical Load at Maximum Supply	Recommended Gate Resistor	Other applications
IRF520N	+/-45V	8 ohm SE	22 ohms	Only for 8 ohm SE Loads
FQP13N10	+/-45V	6 ohm SE	33 ohms	6 ohm BR at +/-25V 8 ohm BR at +/-33V
STP14NF10	+/-45V	6 ohm SE	33 ohms	6 ohm BR at +/-25V 8 ohm BR at +/-33V
IRF530N	+/-45V	4 ohm SE / 8 ohm BR	15 ohms	6 ohm BR at +/-33V
BUK7575-100A	+/-45V	4 ohm SE / 6 ohm BR	15 ohms	4 ohm BR at +/-33V
STP24NF10	+/-45V	4 ohm SE / 6 ohm BR	10 ohms	4 ohm BR at +/-35V
FQP16N15	+/-60V	6 ohm SE / 8 ohm BR	15 ohms	6 ohm BR at +/-45V
FQP19N10	+/-45V	6 ohm SE	33 ohms	6 ohm BR at +/-25V 8 ohm BR at +/-33V
FDP2572	+/-60V	4 ohm SE / 6 ohm BR	15 ohms	4 ohm BR at +/-45V

SE stands for Single Ended Outputs and BR stands for Bridged Output

MOSFETs Under Evaluation

The following MOSFETs appear to be suitable for use with the TP2150B, and we are waiting for samples to evaluate. Most of these devices come from the same “family” or generation, as other recommended MOSFETs. However, experience tells us that we cannot recommend any devices until we have received samples and fully tested them.

**Device Information – MOSFETs Under Evaluation**

Part Number	Manufacturer	BV <sub>DSS</sub> (V)	I <sub>D</sub> (A)	Q <sub>g</sub> (nC)	R <sub>DS(on)</sub> (Ω)	P <sub>D</sub> (W)	Package
FQP14N15	Fairchild Semiconductor	150	14.4	18	.164	104	T0220
FDP3682	Fairchild Semiconductor	100	32	18.5	0.032	95	TO220

Note: The devices are listed in ascending current capability not in order of recommendation.

### Output Filter Design

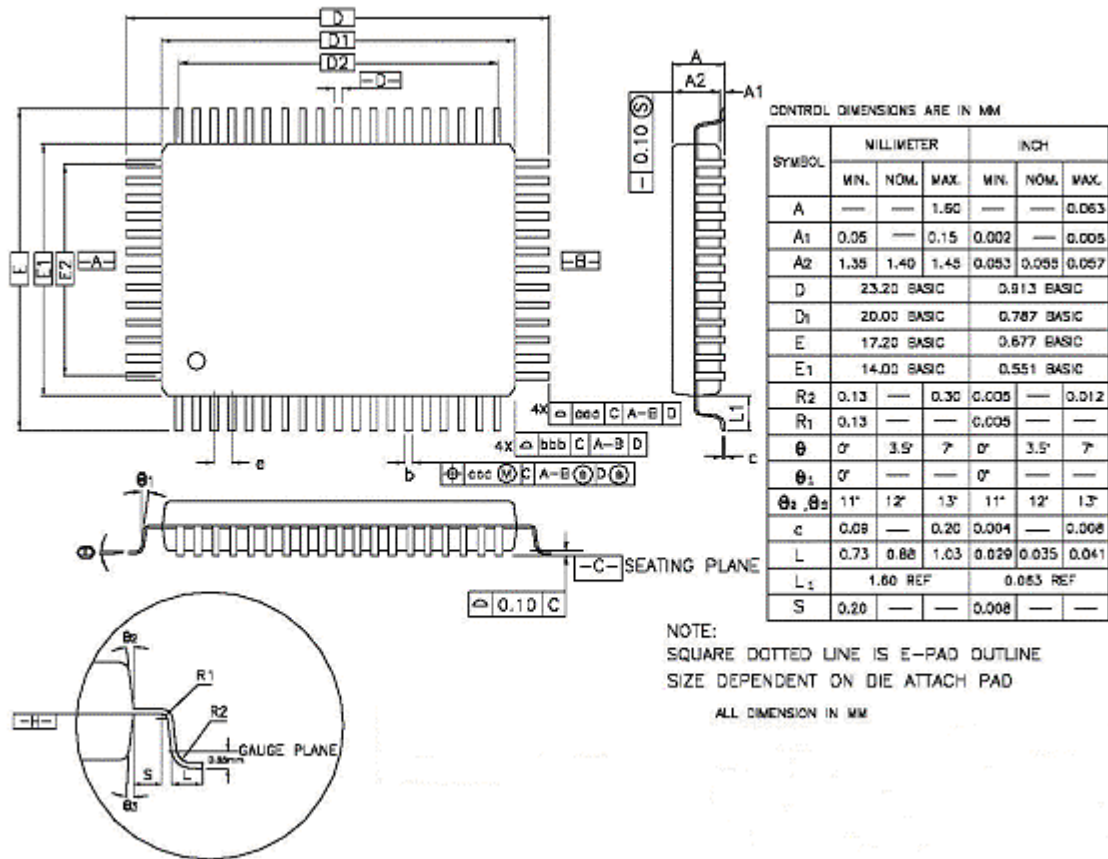
One advantage of Tripath amplifiers over PWM solutions is the ability to use higher-cutoff-frequency filters. This means load-dependent peaking/droop in the 20kHz audio band potentially caused by the filter can be made negligible. This is especially important for applications where the user may select a 6-Ohm or 8-Ohm speaker. Furthermore, speakers are not purely resistive loads and the impedance they present changes over frequency and from speaker model to speaker model.

Tripath recommends designing the filter as a 2nd order, 100kHz LC filter. Tripath has obtained good results with  $L_F = 11\mu\text{H}$  and  $C_F = 0.15\mu\text{F}$  for  $6\Omega$  and  $8\Omega$  loads and  $L_F = 18\mu\text{H}$  and  $C_F = 0.22\mu\text{F}$  for  $4\Omega$  loads.

The core material of the output filter inductor has an effect on the distortion levels produced by a TP2150B amplifier. Tripath recommends low- $\mu$  type-2 iron powder cores because of their low loss and high linearity (available from Micrometals, [www.micrometals.com](http://www.micrometals.com)).

Tripath also recommends that an RC damper be used after the LC low-pass filter. No-load operation of a TP2150B amplifier can create significant peaking in the LC filter, which produces strong resonant currents that can overheat the output MOSFETs and/or other components. The RC dampens the peaking and prevents problems. Tripath has obtained good results with  $R_Z = 20\Omega$  and  $C_Z = 0.15\mu\text{F}$  for  $6\Omega$  and  $8\Omega$  loads and  $R_Z = 15\Omega$  and  $C_Z = 0.22\mu\text{F}$  for  $4\Omega$  loads.

### TP2150B Package Information





## TP2150B Package Information

64-pin LQFP

SYMBOL	64L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.35	0.40	0.50	0.014	0.016	0.020
e	1.00 BSC.			0.039 BSC.		
D2	18.00 REF			0.709 REF		
E2	12.00 REF			0.472 REF		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	—	0.20	—	—	0.008	—

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.  
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE  $\boxed{-H-}$
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.  
ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED.  
THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm.  
DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

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